Abstracts

An agile stored /spl Sigma//spl Delta/ sequence fractional-N synthesiser

R. Walkington and P. Brennan. "An agile stored /spl Sigma//spl Delta/ sequence fractional-N synthesiser." 2001 MTT-S International Microwave Symposium Digest 01.2 (2001 Vol. II [MWSYM]): 697-700 vol.2.

The performance of /spl Sigma//spl Delta/ fractional-N frequency synthesisers has a direct relation to reference frequency. The upper limit on this reference frequency is often caused by the modulator, due to the limited speed achievable in fixed point hardware. Fixed point modulator feedback coefficients with limited precision also reduce modulator cycle length leading to unavoidable periodicity in the modulator output stream. To avoid these problems, a synthesiser has been designed which is particularly suited to burst mode systems such as DCS1800. The prototype described here stores pre-generated /spl Sigma//spl Delta/ sequences in fast memory for each required channel, allowing a 'virtual' /spl Sigma//spl Delta/ modulator operating at 240 MHz to be implemented with a low cost FPGA and flash memory.

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